UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,075	06/15/2001	Marc Donis	A00774/70178 (EJR)	1583

34705 7590 05/24/2007
APRISMA MANAGEMENT TECHNOLOGIES, INC.
273 CORPORATE DRIVE
PORTSMOUTH, NH 03801

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
05/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/883,075	DONIS ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,7-9,11-17,33-39 and 41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,7-9,11-17,33-39 and 41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 and 9 are objected to because of the following informalities:

Claim 1 recites, "**communication units** corresponding to a first quality of service" in line 3-4, "**communication units** corresponding to a first quality of service" in line 5-6, "**communication units**" in line 8, and "**the** communication units" in line 9. It is unclear whether "communication units" in line 8 and "the communication units" in line 9 are the same as "communication units" in line 3-4 or line 5-6.

Claim 9 is also objected for the same reason as set forth above in claim 1.

Claim 1 recites, "**the** first buffer and the second buffer" in line 8. For clarity, it is suggested to revise as "the first buffer memory" and "the second buffer memory".

Claim 9 is also objected for the same reason as set forth above in claim 1.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102 (b)

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 9, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamada (US005581544A).

Regarding Claims 1 and 9, Hamada discloses a switch (see FIG. 1-2; ATM multiplexing apparatus; see col. 2, line 49-50; see col. 6, line 45-55) for a communication network (see FIG. 1, ATM network; see col. 1, line 20-25), the switch comprising:

a plurality of ports (see FIG. 1, interfaces/ports at Mux 12 that couples to different lines 10 (P0-2));

a first buffer memory (see FIG. 2, Highest priority FIFO buffer Q0) having a first queue capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in a buffer, or buffer amount/capacity (i.e. Q0 buffer)) coupled to one of the ports (see FIG. 2, Q0 couple to P0 port) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a first quality of service level (see FIG. 2, storing in priority P0 class of highest QoS; see col. 6, line 56-63; col. 11, line 59-62);

a second buffer memory (see FIG. 2, lower priority FIFO buffer Q1 or Q2) having a second queue capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in buffer, or buffer amount/capacity (i.e. Q1 or Q2 buffer)) coupled to the one of the ports (see FIG. 2, Q1 or Q2 couple to P0 or P1 port) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a second quality of service level (see FIG. 2, storing in priority P1 or P2 class of lower QoS; see col. 6, line 56-63; col. 11, line 59-62); and

a buffer manager (see FIG. 1, a controller 14; see col. 6, line 45-50), coupled to the first buffer memory and the second buffer memory (see FIG. 1, controller 12 couples to Mux 12, which contains Q0 and Q1/2 buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units (see FIG. 2 and FIG. 3, step 1002,1004 with call admitted; see col. 6, line 52-64; see col.

11, line 55-57; QoS of each admitted cell is determined and stores in corresponding Q0, Q1 or Q2 buffer, respectively), and to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 2; see col. 6, line 52-64; each buffered cell are outputted from Q0, Q1 or Q2 buffer, respectively), and

to monitor a measured quality of plurality of network characteristics (see col. 9, line 6-15; QOS parameters such as cell loss rate and delay time) according to a predetermined energy function (see col. 8, line 47 to col. 9, line 25; see col. 11, line 38-48, according to function (e.g. probability distribution function (i.e. normal or Poisson distribution)), the plurality of network characteristics including at least a measure of loss of communication units in the buffer element (see col. 9, line 12-15; see col. 11, line 60-64; see col. 16, line 20-35; measuring loss cells in an ATM mux) and a measure of delay of communication units in the buffer element (see col. 9, line 11-25; col. 9, line 12-15; see col. 11, line 60-64; see col. 16, line 20-35; calculating/evaluating/measuring delay time of for each cells in the ATM switch) to propose adjustments to at lest one of the first capacity and the second capacity by iterative mutation of at lest one of the first capacity and the second capacity (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller suggests/determines/proposes to routinely/repeatedly change/adjust each buffer amount/capacity for each class/QoS by updating buffer amount/capacity);

to adjust a capacity of at least one of the first queue capacity of the first buffer memory or the second queue capacity of the second buffer memory (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller changes/adjusts each buffer amount/capacity for class/QoS by

updating buffer amount/capacity) upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of the network characteristics according to the energy function (see col. 8, line 47 to col. 9, line 25; see col. 11, line 38-48; col. 11, line 59 to col. 12, line 32; according to changes/adjustment that provides buffer amount optimization by measuring QoS parameters according to the function (e.g. distribution function)).

Regarding Claim 33, Hamada discloses a buffer element (see FIG. 1-2; ATM multiplexing apparatus; see col. 2, line 49-50; see col. 6, line 45-55) for a communication network (see FIG. 1, ATM network; see col. 1, line 20-25), the buffer element comprising:

a first buffer memory (see FIG. 2, Highest priority FIFO buffer Q0) having a first capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in a buffer, or buffer amount/capacity (i.e. Q0 buffer)) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a first quality of service level (see FIG. 2, storing in priority P0 class of highest QoS; see col. 6, line 56-63; col. 11, line 59-62);

a second buffer memory (see FIG. 2, lower priority FIFO buffer Q1 or Q2) having a second capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in buffer, or buffer amount/capacity (i.e. Q1 or Q2 buffer)) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a second quality of service level (see FIG. 2, storing in priority P1 or P2 class of lower QoS; see col. 6, line 56-63; col. 11, line 59-62); and

a buffer manager (see FIG. 1, a controller 14; see col. 6, line 45-50), coupled to the first buffer memory and the second buffer memory (see FIG. 1, controller 12 couples to Mux 12, which contains Q0 and Q1/2 buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication

units (see FIG. 2 and FIG. 3, step 1002,1004 with call admitted; see col. 6, line 52-64; see col. 11, line 55-57; QoS of each admitted cell is determined and stores in corresponding Q0, Q1 or Q2 buffer, respectively), to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 2; see col. 6, line 52-64; each buffered cell are outputted from Q0, Q1 or Q2 buffer, respectively), and

monitoring a measured quality of plurality of network characteristics (see col. 9, line 6-15; QOS parameters such as cell loss rate and delay time) according to a predetermined energy function (see col. 8, line 47 to col. 9, line 25; see col. 11, line 38-48, according to function (e.g. probability distribution function (i.e. normal or Poisson distribution)), the plurality of network characteristics including at least a measure of loss of communication units in the buffer element (see col. 9, line 12-15; see col. 11, line 60-64; see col. 16, line 20-35; measuring loss cells in an ATM mux) and a measure of delay of communication units in the buffer element (see col. 9, line 11-25; col. 9, line 12-15; see col. 11, line 60-64; see col. 16, line 20-35; calculating/evaluating/measuring delay time of for each cells in the ATM switch)

determining adjustments to the assigned capacities by iterative mutation of at least one of the assigned capacities (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller suggests/determines/proposes to routinely/repeatedly change/adjust each buffer amount/capacity for each class/QoS by updating buffer amount/capacity); and

to propose adjustments to at lest one of the first capacity and the second capacity by iterative mutation of at lest one of the first capacity and the second capacity (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount

optimization of a controller suggests/determines/proposes to routinely/repeatedly change/adjust each buffer amount/capacity for each class/QoS by updating buffer amount/capacity);

adjusting the assigned capacities of the plurality of buffers (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller changes/adjusts each buffer amount/capacity for class/QoS by updating buffer amount/capacity) upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of the network characteristics according to the energy function (see col. 8, line 47 to col. 9, line 25; see col. 11, line 38-48; col. 11, line 59 to col. 12, line 32; according to changes/adjustment that provides buffer amount optimization by measuring QoS parameters according to the function (e.g. distribution function)).

Regarding Claims 8 and 42, Hamada discloses wherein the communication units are ATM cells (see col. 6, line 55-60; storing ATM cells).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada in view of Irie (US005550823A).

Regarding Claim 43, Hamada discloses a switch (see FIG. 1-2; ATM multiplexing apparatus; see col. 2, line 49-50; see col. 6, line 45-55) for a communication network (see FIG. 1, ATM network; see col. 1, line 20-25), the buffer element comprising:

a plurality of ports (see FIG. 1, interfaces/ports at Mux 12 that couples to different lines 10 (P0-2));

a first buffer memory (see FIG. 2, Highest priority FIFO buffer Q0) having a first capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in a buffer, or buffer amount/capacity (i.e. Q0 buffer)) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a first quality of service level (see FIG. 2, storing in priority P0 class of highest QoS; see col. 6, line 56-63; col. 11, line 59-62);

a second buffer memory (see FIG. 2, lower priority FIFO buffer Q1 or Q2) having a second capacity (see col. 6, line 65 to col. 7 line 4; see col. 11, line 60-67; cell count/capacity in buffer, or buffer amount/capacity (i.e. Q1 or Q2 buffer)) to store communication units (see col. 6, line 55-60; storing ATM cells) corresponding to a second quality of service level (see FIG. 2, storing in priority P1 or P2 class of lower QoS; see col. 6, line 56-63; col. 11, line 59-62); and

a buffer manager (see FIG. 1, a controller 14; see col. 6, line 45-50), coupled to the first buffer memory and the second buffer memory (see FIG. 1, controller 12 couples to Mux 12, which contains Q0 and Q1/2 buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units (see FIG. 2 and FIG. 3, step 1002,1004 with call admitted; see col. 6, line 52-64; see col. 11, line 55-57; QoS of each admitted cell is determined and stores in corresponding Q0, Q1 or Q2 buffer, respectively), to retrieve communication units from the first buffer memory and the

second buffer memory (see FIG. 2; see col. 6, line 52-64; each buffered cell are outputted from Q0, Q1 or Q2 buffer, respectively), and to adjust at least one of the first capacity of the first buffer memory or the second capacity of the second buffer memory (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller changes/adjusts each buffer amount/capacity for class/QoS by updating buffer amount/capacity), based on a total memory available to the switch (see FIG. 3, step 1004; changing/updating according to total available bandwidth; see FIG. 4, total buffer amount L; see col. 11, line 50-56, 59-61), the first and second capacities (see FIG. 4, step 11-2; changing/updating according to buffer amount for class M (i.e. Q0) and class m (i.e. Q1 or Q2); see col. 12, line 7-11), and the quality of service provided by each buffer memory (see col. 11, line 59-65; changing/updating according to QoS of each priority classes buffer);

to adjust a capacity of at least one of the first queue capacity of the first buffer memory or the second queue capacity of the second buffer memory (see FIG. 4, step 1102,1104,1106,1108,1110,1112; see col. 11, line 59 to col. 12, line 32; buffer amount optimization of a controller changes/adjusts each buffer amount/capacity for class/QoS by updating buffer amount/capacity).

Hamada does not explicitly disclose each of the plurality of ports comprises memories. However, Irie teaches a switch (see FIG. 1, ATM switch) comprising a plurality of ports (see FIG. 1, Input circuits 1-N), wherein each of the plurality of ports (see FIG. 1, Input circuit 1) comprises a first buffer memory (see FIG. 1, first Queue 22) having a first capacity to store communication units corresponding to a first quality of service level (see col. 3, line 40-65; logical queue 22 stores cells), and a second buffer memory (see FIG. 1, second queue 22) having

a second capacity to store communication units corresponding to a first quality of service level (see col. 3, line 40-65; a second queue 22 stores higher priority cells). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the plurality of ports comprising buffers/queues, as taught by Irie in the system of Hamada, so that it would perform priority control for cells in the ATM switch of satisfying set loss and delay qualities; see Irie col. 2, line 34-43.

6. Claim 1,2,6-9,11-17,33-37,42 and 43 rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara (US005872769A) in view of Hatono (US 5,737,314).

Regarding Claims 1 and 9, Caldara discloses a switch (see FIG. 1 and 6; ATM switch) for a communication network (see col. 1, line 16-35; in a ATM network), the switch comprising:

a plurality of ports (see FIG. 1, Input ports 0-n 20 and Output port 0-n 22);

a first buffer memory (see FIG. 1-2, first Input/output queue 32/34, FIG. 6, Pri#1 or VBR buffer/queue) having a first queue capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of first Input/output buffer/queue) coupled to one of the ports (see FIG. 1, couple to input/output ports) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a first quality of service level (see FIG. 6, storing in Pri#1 or VBR; see col. 8, line 65 to col. 9, line 40);

a second buffer memory (see FIG. 1-2, second Input/output queue 32/34; FIG. 6, Pri#4 or ABR buffer/queue) having a second queue capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of second Input/output buffer/queue) coupled to the one of the ports (see FIG. 1, couple to

input/output ports) to store communication units corresponding to a second quality of service level (see FIG. 6, storing in Pri#4 or ABR; see col. 8, line 65 to col. 9, line 40); and

a buffer manager (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64), coupled to the first buffer memory and the second buffer memory (see FIG. 1, a combined bandwidth control and Arbiter system couples to first and second priority queues/buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, and to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 1, 6, a combined bandwidth and control system stores/writes/input and retrieves/read/output the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and

monitor a measure of quality of a plurality of network characteristics, the network characteristics including at least a measure of loss of communication units in the buffer element (see col. 6, line 9-20; checking/measuring the error of the received cell in the ATM switch);

to propose adjustments to at least one of the first capacity and the second capacity by iterative mutation of at least one of the first capacity and the second capacity (see col. 7, line 30-65; see col. 8, line 19 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter suggests/determines/proposes to dynamically and routinely/repeatedly manages/adjusts/changes/mutates each queue for dynamic threshold/capacity),

to adjust a capacity of at least one of the first queue capacity of the first buffer memory or the second queue capacity of the second buffer memory (see col. 7, line 30-65; see col. 8, line 19

to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/capacity).

Caldara does not explicitly disclose monitoring according to a predetermined energy function, the plurality of network characteristics including at least a measure of delay of communication units in the buffer element, upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of network characteristic according to the energy function.

However, Hatono teaches monitor a measure of quality of a plurality of network characteristics according to a predetermined energy function (see col. 8, line 5-25, 35-50; testing/measuring the cells loss and delay according to predefined/predetermined density function), the plurality of network characteristics including at least a measure of loss of communication units in the buffer element and a measure of delay of communication units in the buffer element (see col. 8, line 35-60; testing/measuring cells loss and delay of cells in the switch system (FIG. 1)),

to propose adjustments to at least one of the first capacity and the second capacity by iterative mutation of at least one of the first capacity and the second capacity (see col. 6, line 30-67; col. 8, line 35 to col. 9, line 5; suggesting/determining/proposing to routinely/repeatedly update/regulate/reduce the acceptable level/capacity/size);

upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of network characteristic according to the energy function (see col. 6, line 30-67, see col. 6, line 9-30; col. 8, line 15-67; according to suggested/proposed

adjustment/updates/regulation/reducing that provides realistic on testing of cell loss and delay according to the function (e.g. density function)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide disclose monitoring according to a predetermined energy function, the plurality of network characteristics including at least a measure of delay of communication units in the buffer element, upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of network characteristic according to the energy function, as taught by Hatono in the system of Caldara, so that it would provide traffic control function according to test results; see Hatono see col. 6, line 30-67.

Regarding Claim 33, Caldara discloses a buffer element (see FIG. 1 and 6; ATM switch) for a communication network (see col. 1, line 16-35; in a ATM network), the buffer element comprising:

a first buffer memory (see FIG. 1-2, first Input/output queue 32/34, FIG. 6, Pri#1 or VBR buffer/queue) having a first capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of first Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a first quality of service level (see FIG. 6, storing in Pri#1 or VBR; see col. 8, line 65 to col. 9, line 40);

a second buffer memory (see FIG. 1-2, second Input/output queue 32/34; FIG. 6, Pri#4 or ABR buffer/queue) having a second capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of second Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line

18-26; ATM cells) corresponding to a second quality of service level (see FIG. 6, storing in Pri#4 or ABR; see col. 8, line 65 to col. 9, line 40); and

a buffer manager (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64), coupled to the first buffer memory and the second buffer memory (see FIG. 1, a combined bandwidth control and Arbiter system couples to first and second priority queues/buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 1, 6, a combined bandwidth and control system stores/writes/input and retrieves/read/output the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and

monitor a measure of quality of a plurality of network characteristics, the network characteristics including at least a measure of loss of communication units in the buffer element (see col. 6, line 9-20; checking/measuring the error of the received cell in the ATM switch);

determining adjustments to the assigned capacities of at lest one of the assigned capacities (see col. 7, line 30-65; see col. 8, line 19 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter suggests/determines/proposes to dynamically and routinely/repeatedly manages/adjusts/changes/mutates each queue for dynamic threshold/capacity

to propose adjustments to at least one of the first capacity and the second capacity by iterative mutation of at least one of the first capacity and the second capacity (see col. 7, line 30-65; see col. 8, line 19 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined

system of bandwidth control and arbiter suggests/determines/proposes to dynamically and routinely/repeatedly manages/adjusts/changes/mutates each queue for dynamic threshold/capacity),

adjusting the assigned capacities of the plurality of buffers upon determining a proposed adjustment (see col. 7, line 30-65; see col. 8, line 19 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/capacity); see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67.

Caldara does not explicitly disclose monitoring according to a predetermined energy function, the plurality of network characteristics including at least a measure of delay of communication units in the buffer element, upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of network characteristic according to the energy function.

However, Hatono teaches monitoring a measure of quality of a plurality of network characteristics according to a predetermined energy function (see col. 8, line 5-25, 35-50; testing/measuring the cells loss and delay according to predefined/predetermined density function), the plurality of network characteristics including at least a measure of loss of communication units in the buffer element and a measure of delay of communication units in the buffer element (see col. 8, line 35-60; testing/measuring cells loss and delay of cells in the switch system (FIG. 1)),

determining adjustments to assigned capacities by iterative mutation of at least one of the assigned capacities (see col. 6, line 30-67; col. 8, line 35 to col. 9, line 5;

suggesting/determining/proposing to routinely/repeatedly update/regulate/reduce the acceptable level/capacity/size);

upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of network characteristic according to the energy function (see col. 6, line 30-67, see col. 6, line 9-30; col. 8, line 15-67; according to suggested/proposed adjustment/updates/regulation/reducing that provides realistic on testing of cell loss and delay according to the function (e.g. density function)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide disclose monitoring according to a predetermined energy function, the plurality of network characteristics including at least a measure of delay of communication units in the buffer element, upon determining a proposed adjustment that provides an improvement to the measure of quality of the plurality of network characteristic according to the energy function, as taught by Hatono in the system of Caldara, so that it would provide traffic control function according to test results; see Hatono see col. 6, line 30-67.

Regarding Claim 2, Caldara discloses a sorter unit (see FIG. 1, a combined scheduling/sorting system of Switch Allocation Table (SAT) (see FIG. 3) and BA 12) coupled to the first buffer memory and the second buffer memory to selectively store a communication unit in the first buffer or the second buffer based on a quality of service level of the communication unit (see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67; the combined switching system schedules/sorts the ATM cells according to their service classes).

Regarding Claim 7, Caldara discloses the first buffer memory and the second buffer memory are regions of memory in a contiguous random access memory device (see col. 5, line

65 to col. 6, line 4; each TSPP/ includes cell buffer RAM which are organized/contiguous into queues).

Regarding Claims 8, 17 and 42, Caldara discloses wherein the communication units are ATM cells (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells).

Regarding Claim 11, Caldara discloses a plurality of output ports (see FIG. 1, Output port 0-n) that output communication units from the switch to the network (see col. 5, line 35-50; output ports connects the switch 10 to ATM network); and

the first buffer memory and the second buffer memory (see FIG. 1-2, first and second Input queue 32 a-m) are coupled to one of the plurality of output ports (see FIG. 1, Output port 0-n), to store communication units to be output to the one of the plurality of output ports (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; Input queues stores ATM cells to output to output ports).

Regarding Claim 12, Caldara discloses each of the plurality of output ports has a respective first buffer memory (see FIG. 1-2, first output queue 34 a) and a respective second buffer memory (see FIG. 1-2, second output queue 34 m) to store communication units transmitted across the respective output port (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; first and second output queues stores ATM cells which are transmitted to output port).

Regarding Claim 13, Caldara discloses each of the plurality of output ports has a respective buffer manager (see FIG. 1, a control in output port) to selectively store communication units in the respective first buffer and the respective second buffer (see FIG. 1-2, first and second output queue 34 a and m) based on a corresponding quality of service level of

the communication units (see FIG. 6, storing in VBR or ABR output queues; see col. 8, line 65 to col. 9, line 40), and to retrieve communication units from the respective first buffer memory and the respective second buffer memory (see FIG. 1, 6, control processor in the stores/writes/input and retrieves/read/output the cells to/from first and second output queues; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67).

Regarding Claim 14, Caldara discloses a plurality of input ports (see FIG. 1, Input ports 0-n 20) that receive communication units from the switch to the network (see col. 5, line 35-50; input ports receives ATM cells the switch 10 to ATM network); and the first buffer memory (see FIG. 1-2, first output queue 34 a) and the second buffer memory (see FIG. 1-2, first output queue 34 m) are coupled to one of the plurality of input ports (see FIG. 1, Input ports 0-n 20), to store communication units received on the one of the plurality of input ports (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; Output queues 34 stores ATM cells receives from input ports).

Regarding Claim 15, Caldara discloses each of the plurality of input ports (see FIG. 1, Input ports 0-n 20) has a respective first buffer memory (see FIG. 1-2, first Input queue 32 a) and a respective second buffer memory (see FIG. 1-2, second Input queue 32 m) to store communication units transmitted across the respective input port (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; first and second input queues stores ATM cells which are transmitted across input port).

Regarding Claim 16, Caldara discloses each of the plurality of input ports has a respective buffer manager (see FIG. 1, a control in input port) to selectively store communication units in the respective first buffer and the respective second buffer (see FIG. 1-2, first and second

input queue 32 a and m) based on a corresponding quality of service level of the communication unit, and to retrieve communication units from the respective first buffer memory and the respective second buffer memory (see FIG. 1, 6, control processor in the stores/writes/input and retrieves/read/output the cells to/from first and second input queues; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67).

Regarding Claim 34, Caldara discloses wherein the plurality of network characteristics further include one or more of the communication unit processing rate for one of the quality of service levels (see col. 6, line 30-40; see col. 14, line 21-27; switch utilization/processing rate for quality service classes) and the communication unit delay rate for one of the quality of service levels (see col. 1, line 27-50; see col. 2, line 64 to col. 3, line 6; see col. 7, line 40-46; see col. 9, line 21-40; see col. 13, line 33-40; delay bound/parameter/rate for service class priorities).

Regarding Claims 35 and 36, Caldara discloses each of the plurality of buffers (see FIG. 1-2, and 6; Input/output queues 32/34) stores communication units for a single port wherein the single port is an output put (see FIG. 1 and 6, Output port 0) in a communication network switch (see FIG. 1,2,6; ATM switch 10); see col. 4, line 50-65; col. 8, line 65 to col. 9, line 40.

Regarding Claims 37, Caldara discloses wherein the plurality of buffers (see FIG. 1-2, and 6; Input/output queues 32/34) stores the communication units for each port of a switch in the communication network (see FIG. 1 and 6, Input or Output port 0-n); see col. 4, line 50-65; col. 8, line 65 to col. 9, line 40.

7. Claims 5 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara and Hatono, and further in view of Holender (US006069894A).

Regarding Claims 5 and 41, the combined system of Caldara and Hatono discloses iterative mutation of at least one of the first capacity and the second capacity as described above in claim 1 and 33.

Neither Caldara nor Hatono explicitly disclose a steepest ascent hill-climbing search. However, Holender further teaches means for performing a steepest ascent hill-climbing search (see col. 5, line 42-46; see col. 13, line 39-60; col. 16, line 10 to col. 17, line 27; ascend or step hill climbing process is used to search possible assignment/value to determine optimize threshold/value). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide hill climbing search process, as taught by Holender in the combined system of Caldara and Hatono, so that it would avoid overload situation and provide load balancing in accordance with optimization method; see Holender col. 16, line 9-16; see col. 17, line 33-37; see col. 4, line 10-64.

8. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara and Hatono, and further in view of Kakuma (US005555265A).

Regarding Claim 38, the combined system of Caldara and Hatono discloses determining a priority level for communication units for each of the quality of service levels as described above in claim 33.

Neither Caldara nor Hatono explicitly disclose level for dropped. However, Kakuma teaches determining a priority level for dropped communication units for each of the quality of service levels (see col. 5, line 33-67; determining discard priority for each quality class). Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to provide determining discard priority for each quality class, as taught by Kakuma in the combined system of Caldara and Hatono, so that it would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15.

Regarding Claim 39, the combined system of Caldara and Hatono discloses determining a priority level for communication units for each of the quality of service levels as described above in claim 33.

Neither Caldara nor Hatono explicitly disclose delay for quality service level. However, Kakuma teaches determining a priority level for communication unit's delay for each of the quality of service levels (see col. 14, line 45-65; see col. 15, line 20-34; determining delay priority for each quality class). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide determining delay priority for each quality class, as taught by Kakuma in the combined system of Caldara and Hatono, so that it would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15.

9. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Caldara in view of Irie (US005550823A).

Regarding Claim 43, Caldara discloses Caldara discloses a buffer element (see FIG. 1 and 6; ATM switch) for a communication network (see col. 1, line 16-35; in a ATM network), the buffer element comprising:

a first buffer memory (see FIG. 1-2, first Input/output queue 32/34, FIG. 6, Pri#1 or VBR buffer/queue) having a first capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of first Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a first quality of service level (see FIG. 6, storing in Pri#1 or VBR; see col. 8, line 65 to col. 9, line 40);

a second buffer memory (see FIG. 1-2, second Input/output queue 32/34; FIG. 6, Pri#4 or ABR buffer/queue) having a second capacity (see col. 4, line 45-65; see col. 6, line 30-65; see col. 7, line 30-60; see col. 8, line 52 to col. 9, line 40; bandwidth threshold/capacity of second Input/output buffer/queue) to store communication units (see col. 1, line 16-35; see col. 8, line 18-26; ATM cells) corresponding to a second quality of service level (see FIG. 6, storing in Pri#4 or ABR; see col. 8, line 65 to col. 9, line 40); and

a buffer manager (see FIG. 1, a combined system of control in To/From Switch Port Processor 14/16 and Bandwidth Arbiter (BA) 12; see col. 4, line 32-64), coupled to the first buffer memory and the second buffer memory (see FIG. 1, a combined bandwidth control and Arbiter system couples to first and second priority queues/buffers), to selectively store communication units in the first buffer and the second buffer based on a corresponding quality of service level of the communication units, to retrieve communication units from the first buffer memory and the second buffer memory (see FIG. 1, 6, a combined bandwidth and control system stores/writes/input and retrieves/read/output the cells to/from first and second priority queues/buffers; see col. 4, line 32 to col. 6, line 29; see col. 8, line 50 to col. 10, line 67), and to adjust at least one of the first capacity of the first buffer memory or the second capacity of the

second buffer memory (see col. 7, line 30-65; see col. 8, line 19 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67; the combined system of bandwidth control and arbiter dynamically manages/adjusts each queue for dynamic threshold/capacity), based on a total memory available to the switch (see FIG. 7, total bandwidth available (i.e. total of used & unused bandwidth threshold), the first and second capacities (see FIG. 7, used bandwidth thresholds/capacities by the queues), and the quality of service provided by each buffer memory (see col. 9, line 1-40; service quality of each queue); see col. 7, line 30-65; see col. 8, line 52 to col. 9, line 34; see col. 9, line 64 to col. 10, line 67.

Caldara does not explicitly disclose each of the plurality of ports comprises memories. However, Irie teaches a switch (see FIG. 1, ATM switch) comprising a plurality of ports (see FIG. 1, Input circuits 1-N), wherein each of the plurality of ports (see FIG. 1, Input circuit 1) comprises a first buffer memory (see FIG. 1, first Queue 22) having a first capacity to store communication units corresponding to a first quality of service level (see col. 3, line 40-65; logical queue 22 stores cells), and a second buffer memory (see FIG. 1, second queue 22) having a second capacity to store communication units corresponding to a first quality of service level (see col. 3, line 40-65; a second queue 22 stores higher priority cells). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide each of the plurality of ports comprising buffers/queues, as taught by Irie in the system of Caldara, so that it would perform priority control for cells in the ATM switch of satisfying set loss and delay qualities; see Irie col. 2, line 34-43.

Response to Arguments

10. Applicant's arguments filed 2-9-07 have been fully considered but they are not persuasive.

Regarding claims 1,2,5,7-9,11-17,33-39 and 41-43, the applicant argued that, "...neither Caldara alone or in combination...discloses, teach or suggest all of the features of the claimed invention...claim 1 recites: "a buffer manager...to adjust at least one of the first capacity of the first buffer memory or the second capacity of the second buffer memory...Caldara fails to disclose adjusting buffer capacities..." in page 9.

In response to applicant's argument, the examiner respectfully disagrees with the argument since the combined system of Caldara and Hatono discloses the claimed invention as set forth above in rejection of claim 1,9,33, and 43.

Moreover, Caldara discloses as follows:

By implementing this overall "list of lists" structure in the presently disclosed ATM switch, multiple levels of control are provided. For instance, the first time an event occurs which enables one cell to be transmitted to Port 0.sub.3, a cell from the first cell in the first queue associated with scheduling list 12 will be selected. This is cell C1 of Queue 3. **The pointers of the "Dynamic Bandwidth Lists" list and SLISTs 12 and 5 are adjusted such that SLIST 2 is the next scheduling list from which a cell is provided if dynamic bandwidth becomes available for transmission of a cell to output Port 0.sub.3. SLIST 5 would be second, and SLIST 12 would then be last**. Similarly, Queue 3, having just provided a cell, becomes the last queue to be eligible to provide a cell vis a vis SLIST 12, with Queue 11 being the next. This occurs through the manipulation of pointers in SLIST 12 and Queues 3 and 11. Finally, cell C1, having been transmitted, is dequeued from Queue 3, meaning the pointers of Queue 3 are readjusted to point to C2 as next to be transmitted. Only if another cell is received into Queue 3 will another cell fall in to line behind cell 4. (see col. 8, line 19-37).

Each queue for each connection has a dynamic bandwidth threshold 37 associated therewith, as shown in FIG. 4. If a queue buffer depth exceeds the cell depth indicated by the respective dynamic bandwidth threshold 37, the scheduling list for that queue will be added to the appropriate dynamic bandwidth list corresponding to the appropriate output port and priority. For each output port, the dynamic bandwidth list provides an indication of which if any cells are to be transmitted to the respective output port using dynamic bandwidth. The dynamic bandwidth threshold is established at call setup time. In a further embodiment of the present switch, however, **the threshold value is adjusted dynamically based upon an empirical analysis of traffic through the switch**.

With regard to FIG. 7, a dynamic bandwidth threshold for a queue of CBR cells, or cells requiring a dedicated bandwidth, would be established such that the requested bandwidth (labelled "A" in FIG. 7) meets or exceeds the requirement. For other applications which may be more bursty but which still require tightly bounded delay, **a dynamic bandwidth threshold such as that labelled "B" in FIG. 7 may be suitable, wherein the majority of the traffic is handled by allocated bandwidth, with momentary bursts handled by high-priority dynamic bandwidth**. In either case, bandwidth specifically allocated but unused is made available to the BA by the TSPP for dynamic bandwidth allocation.

Note that for categories of service which rely solely on allocated bandwidth, **the dynamic bandwidth threshold is set above any expected peaks in cell reception.** Conversely, for categories of service having no (or low) delay bounds and no guaranteed bandwidth, such as UBR, **the dynamic bandwidth threshold is set to zero**. (see col. 9, line 6-40) (Emphasis added)

In view of above, it is clear that **"dynamic bandwidth threshold"** value for each priority queue is dynamically adjusted.

Regarding claims 1,2,5,7-9,11-17,33-39 and 41-43, the applicant argued that, "...Hamada fails to discloses...claim 1 recites: "a buffer manager...to adjust at least one of the first capacity of the first buffer memory or the second capacity of the second buffer memory...claim 9 and 33 includes similar features...The portion of Hamada relied upon by the examiner do not discloses a buffer manager that monitors a measure of quality of a plurality of network characteristic according to an energy function. Nor do these portions Hamada discloses adjusting...according to the energy function...Rather, Hamada deals with calculating "a probability distribution"..." in page 10-11.

In response to applicant's argument, the examiner respectfully disagrees with the argument since Hamada discloses the claimed invention as set forth above in rejection of claim 1, 9, 33 and 43.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **any**

specificity of "energy function") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, examiner asserts the Hamda's function as applicant "energy function" as set forth in rejection above.

Regarding claims 5,38,39, and 41, the applicant argued that, "...examiner has failed to provide proper motivation to combined Holander or Kakuma with Caldara..." in page 11-12.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, **(for claim 5 and 41),** it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide hill climbing search process, as taught by Holender in the combined system of Caldara and Hatono, so that it would avoid overload situation and provide load balancing in accordance with optimization method; see Holender col. 16, line 9-16; see col. 17, line 33-37; see col. 4, line 10-64.

In this case, **(for claim 38),** it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide determining discard priority for each quality class, as taught by Kakuma in the combined system of Caldara and Hatono, so that it

would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15

In this case, **(for claim 39),** it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide determining delay priority for each quality class, as taught by Kakuma in the combined system of Caldara and Hatono, so that it would prevent each service from adversely affecting other service and allow the quality of service to be easily controlled; see Kakuma col. 3, line 10-15.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ian N. Moore
Art Unit 2616

5-14-07

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600